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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,230	09/09/2003	Shih-Chang Lee	LEES3021/EM	8848

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EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,230	LEE ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-16 and 21-28* is/are rejected.

7)☒ Claim(s) *2-6 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-28** are pending in this application is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in TAIWAN, 091133275 on 11/13/2002.

Specification

The disclosure is objected to because of the following informalities:

On page 5, paragraph [0023], line 9, the reference numeral "322" in the "a first bonding pads 322" should read –321a--, line 10, the reference numeral "324" in the "a second bonding pads 324" should read –321b--, and the reference numeral "321a" in the "a plurality of first bumps 321a" should read –331--, line 11, the reference numeral "322" in the "the first bonding pads 322" should read –321a--, and the reference numeral "321b" in the "a plurality of second bumps 321b" should read –332--, and line 12, the reference numeral "324" in the "the second bonding pads 324" should read –321b--, and on page 7, line 1, the reference numeral "31" in the "the chip 31" should read –32--.

Claim Objections

Claims **1 and 15** are objected to because of the following reasons.

The "comprising" is missing in the preamble "A flip chip package."

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims **1 and 7, 8 and 10-12** are rejected under 35 U.S.C. 102(a) as being anticipated by Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro").

Regarding claim **1**, Fusaro discloses in Figs. 1-1A and 5 and related texts as set forth in column 3, lines 5-51, and column 6, lines 8-50,

a flip chip package (55):

a lead frame having a die paddle/a planar metal die pad (11) and a plurality of leads (14) surrounding the die paddle/the planar metal die pad,

a chip/a flip chip IC device (56) having an active surface/a lower second surface (58) and a back surface/a upper first surface (57) opposed to the active surface/the lower second surface,

wherein the active surface/the lower second surface has a first bonding pad/bond pads (23) and a second bonding pad/bond pads (23);

and

a plurality of first bumps/solder balls (62) and second bumps/solder balls (62) formed on the first bonding pads/bond pads, and the second bonding pads/bond pads respectively, the active surface/the lower second surface of the chip/the flip chip IC device facing the lead frame and electrically connecting the die paddle/the die pad and the leads by the first bumps/the solder balls and the second bumps/the solder balls respectively.

Regarding claim **7**, Fusaro discloses in Fig. 5 the flip chip package of claim **1**, wherein the first bumps/solder balls are electrically conductive bumps (col. 6, lines 42-43).

Regarding claim **8**, Fusaro discloses in Fig. 5 the flip chip package of claim **1**, wherein the second bumps/solder balls are electrically conductive bumps (col. 6, lines 42-43).

Regarding claim **10**, Fusaro discloses in Fig. 5 the flip chip package of claim **1**, wherein the first bumps/the solder balls are solder bumps (col. 6, line 44).

Regarding claim **11**, Fusaro discloses in Fig. 5 the flip chip package of claim **1**, wherein the second bumps/the solder balls are solder bumps (col. 6, line 44).

Regarding claim **12**, Fusaro discloses in Fig. 5 the flip chip package of claim **1**, further comprising an underfill/an encapsulant material (25) filled in a gap between the active surface/the lower second surface of the chip and the lead frame (col. 3, line 8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim **9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Lo et al. (USP: 6,282,094 hereinafter referred to as "Lo").

Fusaro discloses the all claimed limitations except for the flip chip package of claim **1**, wherein the first bumps are thermally conductive bumps. Lo teaches in Fig. 1 that the BGA IC

package comprises the thermally-conductive solder balls (318) to enhance the overall heat-dissipation efficiency as set forth in column 4, lines 23-25. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the thermally-conductive solder balls, as taught by Lo, to incorporate into Fusaro's structure/package to arrive the claimed invention in order to increase and enhance the overall heat-dissipation efficiency.

Claim **13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Corisis (USP: 6,314,639).

Fusaro discloses the all claimed limitations except for the flip chip package of claim **1**, further comprising a heat spreader mounted on the back surface of the chip. Corisis teaches in Figs. 4 and 5 that each semiconductor device (40) has a heat spreader (52), having an exposed surface (54) for dissipating heat generated in the semiconductor device, mounted on the back surface of the semiconductor die (20) (col. 4, lines 22-26). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a heat spreader mounted on the back of the semiconductor die, as taught by Corisis, to incorporate into Fusaro's structure/package to include a heat spreader mounted on the back of the semiconductor die to form the claimed invention in order to provide high heat dissipation (col. 4, lines 35-36).

Claim **14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Akasaki et al. (USP: 5,217,922 hereinafter referred to as "Akasaki").

Fusaro discloses the all claimed limitations except for the flip chip package of claim **1**, further comprising a heat transmission layer disposed on the back surface of the chip. Akasaki teaches in Fig. 1 that a semiconductor device comprises a heat conducting/transmitting layer (10) disposed on a semiconductor chip (1) to transmit heat which is generated by the operation of each logical circuit mounted on the chip to a sealing cap (3) in high efficiency as set forth in column 5, lines 10-16. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a heat conducting/transmitting layer mounted on the back of the semiconductor die, as taught by Akasaki, to incorporate into Fusaro's structure/package to include the heat conducting/transmitting layer mounted on the back of the semiconductor die to form the claimed invention in order to gain high efficiency heat transmission.

Claims **15, 16, 21, 22 and 24-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Liang (USP: 5,378,924).

Regarding claim **15**, Fusaro discloses in Figs. 1-1A and 5 and related texts as set forth in column 3, lines 5-51, and column 6, lines 8-50,

a flip chip package (55):

a lead frame having a die paddle/a planar metal die pad (11), a plurality of leads (14) surrounding the die paddle/the planar metal die pad;

a chip/a flip chip IC device (56) having an active surface/a lower second surface (58) and a back surface/a upper first surface (57) opposed to the active surface/the lower second surface,

wherein the active surface/the lower second surface has a first bonding pad/bond pads (23) and a second bonding pad/bond pads (23);

and

a plurality of first bumps/solder balls (62) and second bumps/solder balls (62) formed on the first bonding pads/bond pads and the second bonding pads/bond pads respectively, wherein the active surface/the lower second surface of the chip/the flip chip IC device faces the lead frame and electrically connects the die paddle/the die pad and the leads by the first bumps/the solder balls and the second bumps/the solder balls respectively.

Fusaro fails to teach or suggest a tie bar connected to the die paddle and wherein the active surface of the chip faces the lead frame and electrically connects the tie bar by the first bumps.

However, Liang teaches in Fig. 5 that a lead frame (60) has tie bars (61a-61d) connected to the die-attach paddle (62) as set forth in column 5, lines 33-40.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a lead frame has tie bars connected to the die-attach paddle, as taught by Liang, to incorporate into Fusaro's structure/package to have a lead frame having tie bars connected to the die-attach paddle to enhance support of the lead frame and therefore the active surface/the lower second surface of the chip/the flip chip IC device faces the lead frame and electrically connects the tie bar by the first bumps/solder balls.

Regarding claim **16**, Fusaro discloses the all claimed limitations except for the flip chip package of claim **15**, wherein the tie bar further comprises a first concavity formed thereon. Liang teaches in Fig. 5 that a lead frame (60) has a first concavity/locating holes (68a-68d)

formed into the tie bars (61a-61d) connected to the die-attach paddle (62) as set forth in column 5, lines 33-40. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the tie bar further comprises a first concavity/locating holes, as taught by Liang, to incorporate into Fusaro's structure/package to form the claimed invention in order to clip or fixedly attach the lead frame to the elongated stubs and to eliminate reliability problems associated with pad tilting (col. 3, lines 8-10).

Regarding claim **21**, Fusaro discloses in Fig. 5 the flip chip package of claim **15**, wherein the first bumps/solder balls are electrically conductive bumps (col. 6, lines 42-43).

Regarding claim **22**, Fusaro discloses in Fig. 5 the flip chip package of claim **15**, wherein the second bumps/solder balls are electrically conductive bumps (col. 6, lines 42-43).

Regarding claim **24**, Fusaro discloses in Fig. 5 the flip chip package of claim **15**, wherein the first bumps/the solder balls are solder bumps (col. 6, line 44).

Regarding claim **25**, Fusaro discloses in Fig. 5 the flip chip package of claim **15**, wherein the second bumps/the solder balls are solder bumps (col. 6, line 44).

Regarding claim **26**, Fusaro discloses in Fig. 5 the flip chip package of claim **15**, further comprising an underfill/an encapsulant material (25) filled in a gap between the active surface/the lower second surface of the chip and the lead frame (col. 3, line 8).

Claim **23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Liang (USP: 5,378,924) and further in view of Lo et al. (USP: 6,282,094 hereinafter referred to as "Lo").

Fusaro and Liang disclose the all claimed limitations except for the flip chip package of claim **15**, wherein the first bumps are thermally conductive bumps. Lo teaches in Fig. 1 that the BGA IC package comprises the thermally-conductive solder balls (318) to enhance the overall heat-dissipation efficiency as set forth in column 4, lines 23-25. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the thermally-conductive solder balls, as taught by Lo, to enhance the overall heat-dissipation efficiency.

Claim **27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Liang (USP: 5,378,924) and further in view of Corisis (USP: 6,314,639).

Fusaro and Liang disclose the all claimed limitations except for the flip chip package of claim **15**, further comprising a heat spreader mounted on the back surface of the chip. Corisis teaches in Figs. 4 and 5 that each semiconductor device (40) has a heat spreader (52), having an exposed surface (54) for dissipating heat generated in the semiconductor device, mounted on the back surface of the semiconductor die (20) (col. 4, lines 22-26). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a heat spreader mounted on the back of the semiconductor die, as taught by Corisis, in order to provide high heat dissipation (col. 4, lines 35-36).

Claim **28** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fusaro et al. (USP: 6,331,451 hereinafter referred to as "Fusaro") in view of Liang (USP: 5,378,924) and further in view of Akasaki et al. (USP: 5,217,922 hereinafter referred to as "Akasaki").

Fusaro and Liang disclose the all claimed limitations except for the flip chip package of claim **15**, further comprising a heat transmission layer disposed on the back surface of the chip. Akasaki teaches in Fig. 1 that a semiconductor device comprises a heat conducting/transmitting layer (10) disposed on a semiconductor chip (1) to transmit heat which is generated by the operation of each logical circuit mounted on the chip to a sealing cap (3) in high efficiency as set forth in column 5, lines 10-16. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include a heat conducting/transmitting layer mounted on the back of the semiconductor die, as taught by Akasaki, in order to gain high efficiency heat transmission.

Allowable Subject Matter

Claims **2-4, 5-6 and 17-20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations.

Regarding claims **2-4**, Fusaro, Lo, Corisis, Akasaki and Liang, taken alone or in combination, fail to teach the claimed limitation the flip chip package of claim **1**, wherein the die paddle further comprises a first concavity formed thereon and connects to one of the first bumps as recited in claim **2**.

Regarding claims **5 and 6**, Fusaro, Lo, Corisis, Akasaki and Liang, taken alone or in combination, fail to teach the claimed limitation the flip chip package of claim **1**, wherein one of the leads has a second concavity connecting to one of the second bumps as recited in claim **5**.

Regarding claims **17 and 18**, Fusaro, Lo, Corisis, Akasaki and Liang, taken alone or in combination, fail to teach the claimed limitation the flip chip package of claim **16**, wherein one of the first bumps connects the first concavity and one of the first bonding pads as recited in claim **17**.

Regarding claims **19 and 20**, Fusaro, Lo, Corisis, Akasaki and Liang, taken alone or in combination, fail to teach the claimed limitation the flip chip package of claim **15**, wherein one of the leads has a second concavity connecting one of the second bumps as recited in claim **19**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

AH

February 12, 2004

Andy Huynh

Patent Examiner